What is Jitter?

Simply stated, jitter is just noise. The noise causes an uncertainty in the relative position of each clock cycle. In clock and timing circuits, jitter is generated from a number of sources including oscillator noise, PLL noise, power supply variation, output circuit noise, duty cycle, etc.

The picture below shows multiple overlapped clock periods illustrating the non-ideal placement in time of each rising edge. In an ideal signal, each edge would overlap exactly on top of the other, producing an infinitely thin line. In the expanded view below, we can see that the rising edge shows a measurable amount of displacement. This horizontal displacement is jitter.

Why is Jitter Important?

All digital circuits require at least one, and often several clocks for processing and handling data. These timing references can be the clock reference for as few as a handful of synchronous logic blocks to system chipsets incorporating billions of transistors. As gate count and processing speeds increase, chipset designers must
take into account factors such as propagation delay, skew, rise/fall times, etc to ensure adequate margins for proper operation. Jitter is one such factor. It adds uncertainty to the exact timing of an external reference clock.

**Jitter takes Many Forms**

Because clock jitter is nothing more than the time variation between the edge of a clock signal and its ideal location in time, most engineers can intuitively relate to the basic definition of jitter. However, the effect of jitter on the performance of a system is largely dependent on the functional requirements of the application. A more detailed understanding of the makeup of jitter is important in accessing how jitter degrades system performance. To help the system designer, several different methods for specifying and measuring jitter have been developed.

**Period Jitter**

Period jitter is the time difference between measured clock periods.

Period jitter is measured in the time domain and is expressed as either the rms or peak to peak of the time variation.

The period jitter measurement is independent of the clock frequency. Therefore, a very fast clock with a very short period may have the same Period Jitter as that of a very slow clock. For example, a clock with a period of 500ps and 100ps of period jitter would be an extremely noisy clock. The same period jitter on a clock with a 1ms period would be ultra quiet. Comparing the period jitter of two different clock frequencies would therefore be an apple to oranges comparison.

Period jitter is important for determining timing margins in many digital computing systems. For example, a microprocessor may require a specific amount of time for data to be clocked through various internal pipelined stages. Excessive jitter on the clocking
signal may result in a period too short to allow for proper data processing resulting in improper circuit operation. Period jitter is also important for applications such as Analog to Digital Converters that rely on sampling of a continuous signal by a clock. Period jitter translates to aperture uncertainty in determining the actual sampled information.

**Cycle-to-Cycle Jitter**

Cycle-to-Cycle Jitter is the time difference between *adjacent* clock periods.

![Diagram of Cycle-to-Cycle Jitter](image)

\[
\text{Cycle-to-Cycle Jitter} = t_1 - t_2
\]

As with period jitter, Cycle-to-Cycle Jitter is independent of frequency. Because only adjacent cycles are of concern, Cycle-to-Cycle Jitter measures only very short term jitter. The effects of low frequency changes in the clock are minimized such that a gradual frequency modulated clock such as a spread spectrum clock may also have low cycle-to-cycle jitter. Cycle to cycle jitter emphasizes only higher frequency noise components. Cycle to Cycle jitter should always be specified as the maximum difference between the two adjacent clocks (peak value).

Cycle to Cycle jitter is important when analyzing setup and hold time margins of pipelined digital circuits. In these circuits, the short term relationship between data and the clock is important. Variations in the temporal position of the clock with respect to the data may result in violations of setup and hold time specifications and the introduction of erroneous data into the data path.

**Long Term Jitter**

Long Term Jitter is defined as the variation in the time difference between the edge of a reference clock and the same edge of the clock delayed n clock cycles. It includes the net accumulation of jitter over a predefined time, typically 1,000 clock periods. Hence, long term jitter includes low frequency components in its measurement.
Long Term Jitter is important in understanding the net timing margins when jitter is allowed to accumulate over time. If the clock jitter were truly random, the long term jitter would be similar to the period jitter. However, because of non-random deterministic components that cannot be effectively averaged over the 1000 clock cycle period, long term jitter can be significantly larger than period jitter.

Accumulated jitter is particularly important in applications where long chains of sequential data must be observed. Applications that are sensitive to accumulated long term jitter include video displays, FIFO memory, and high speed data transmission to name a few.

![Picture of blurred screen](image)

Take the classical example of an analog TV. Because the picture is painted horizontally line by line, long term jitter may cause lines to be horizontally skewed in time relative to the previous line. The result is a blurry screen with artifacts that reduce the crispness and details of sharp edges. In the picture above, jitter artifacts can be seen on the white painted lines.

**Time Interval Error**

Time Interval Error is the time difference between the measured rising or falling edge of a clock and its ideal position in time at a given frequency. TIE is typically measured over thousands of periods and is displayed as a graph where the vertical axis represents the magnitude of the TIE of each period and the horizontal axis is time.
Unlike period, cycle-to-cycle, or long term jitter, Time Interval Error (TIE) is frequency dependent. This is because each (rising) edge of the measured signal is compared to its ideal location in time. Without an ideal reference to which comparisons can be made, TIE would quickly accumulate to increasingly large values.

Note that TIE is an accumulation of consecutive cycle-to-cycle jitter. This is identical to the definition of Long Term Jitter. In fact, TIE is a continuous measure of Long Term Jitter. Compare the measurement of LTJ over 2us below. Measured in this fashion, LTJ is 9.08ns.

Tracking TIE over the time same time period (ie. 2us) shows TIE starting from the left with zero error and progressing to the right, gradually accumulating errors over time. Overlaying multiple TIE plots and measuring the difference between the minimum and maximum excursion (horizontal cursors) results in a maximum TIE difference of 9.04ns, very close to the results obtained earlier.
The measurement below is a single TIE track of a clock spanning 16,000 periods. Long Term Jitter over this time frame (200us) shows 2.4ns of error. But notice that the two extremes actually occurred within ~20us of each other, indicating that LTJ measured over a 10x shorter duration would not show any improvement.

With a contiguous data track it is now easily to observe changes in the direction of accumulated error. Because accumulation is a gradual phenomenon, we can see in the above data track that a sudden and abrupt change in frequency occurred at each point where the slope inverted. It is easy to observe that the jitter error continues to
accumulate until another frequency shift causes the phase accumulation to reverse direction.

TIE is a power tool. The advantage of TIE over the more traditional jitter measurements as described above is that TIE captures the “how” and “why” of jitter rather than just the end result. TIE allows the engineer to analyze the signal in much greater detail, making this the “king” of all time domain jitter analysis. It allows the engineer to think in the phase frequency domain, yet stay within the time domain.

**Integrated Phase Noise Jitter**

Integrated Phase Noise Jitter differs from the other methods of defining jitter in that it is measured in the frequency domain. The phase noise is the short term fluctuation of the clock edge in the frequency domain. The frequency spectrum of phase noise relative to the clock is plotted below.

By expressing the noise as a function of its frequency components, system analysis can be undertaken where the detailed frequency responses of the actual circuit blocks can be applied to understand how the overall system is affected by the phase noise. The integrated phase noise jitter is the integration of all the phase noise across a given frequency band. Integrated phase noise jitter must be specified over a band of interest. In the frequency domain, deterministic noise sources manifest as discrete frequency components (spurs). As one would expect, integrated phase noise jitter is an important method for measuring jitter in communication systems.
As an example of how a system designer might use a phase noise plot to analyze system jitter, let’s examine the response of a clock used as the reference to a Phase Locked Loop (PLL). In the PLL block diagram below, the operation of the circuit forces the output of the Divider block to be the same frequency and phase as the Reference Clock at the input of the Phase Frequency Detector.

The PLL has a bandwidth determined by the parameters of the PFD, Loop Filter & Voltage Controlled Oscillator (VCO). The transfer function of the Reference Clock to the output of the VCO is equivalent to a low pass filter function where the -3db point is the PLL bandwidth. Any frequency components of the Reference Clock below the PLL bandwidth pass thru to the output while higher frequency components above the PLL bandwidth are attenuated. This example demonstrates how a PLL can be employed to “clean” a noisy clock.

Phase Noise is a complicated topic and is beyond the scope of this paper.

Summary

The impact of jitter can vary widely from one application to another. Because jitter takes many forms, it is important for the engineer to understand which jitter measurement or combination of measurements are most appropriate for his system. With a strong understanding of jitter, system margins can be improved with higher reliability, increased flexibility and ultimately enabling higher performance at reduced costs.